The TDCpix readout ASIC: a 75 ps resolution timing front-end for the Gigatraceker of the NA62 experiment


CERN European Organization for Nuclear Research
NA62 Collaboration
Outline

Introduction
- NA62 Gigatracker
- TDCpix readout ASIC

Design of TDCpix
- Architecture
- Front-End
- TDC

Prototype ASIC
- Measured performances
NA62 experiment and Gigatracker

NA62 experiment at CERN SPS
- Direct measurement of rare decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$
- In flight decay of Kaons from a high rate (~1 GHz) hadron beam

Gigatracker: Kaon spectrometer
- 150 ps resolution time stamping, 200 ps for each station
- Follow talk by M. Fiorini, 10-Jun-2011, 14:20
Detector geometry and beam profile

Total particle rate 1 GHz

Peak beam intensity 1.73 MHz/mm$^2$
TDCpix block diagram

Requirements

- 45 x 40 pixel channels
  300 x 300 μm²
- Chip hit rate
  ~130 MHz
- Timing resolution
  200 ps RMS
- Readout efficiency
  98 %
- Power budget
  2 W/cm²

Architecture

- Analog pixel matrix, digital EoC
- Transmission lines send discriminated hits to EoC
- Data driven, trigger-less
- Data output: 4x 2.4 Gb/s
- IBM CMOS 130 nm, 1.2V, 8 Metal layers
Pixel cell

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range</td>
<td>0.6-10 fC / 3600-60000 e-</td>
</tr>
<tr>
<td>Gain</td>
<td>75 mV/fC</td>
</tr>
<tr>
<td>Peaking time</td>
<td>5 ns</td>
</tr>
<tr>
<td>ENC (no sensor)</td>
<td>130 e-</td>
</tr>
<tr>
<td>FE power</td>
<td>130 μA (56%)</td>
</tr>
<tr>
<td>TX line driver</td>
<td>100 μA (44%)</td>
</tr>
<tr>
<td>Full matrix power</td>
<td>500 mW</td>
</tr>
</tbody>
</table>
Pixel cell

Circuits occupy half of pixel area
- Half column for transmission lines

Layout focus on immunity to noise
- Full separation of pixel matrix from EoC circuitry
- Analog section inside isolated implant well
- Front-end transistors in triple wells
TDC

45x40 pixel matrix

End of Column

TDC TDC TDC

Readout Readout Config Readout Readout

TDC
Time walk and Time Over Threshold

\[ t_{\text{lead}} \quad t_0 \quad t_{\text{trail}} \]

A.u.

Thr.

\[ t_{\text{lead}} \quad \text{ToT} \quad t_{\text{trail}} \]

\[ t [\text{ns}] \]

\[ \times 10^{-9} \]

\[ 52 \quad 50 \quad 48 \quad 46 \quad 44 \quad 42 \quad 40 \quad 38 \quad 36 \quad 34 \quad 32 \]

\[ 2 \quad 4 \quad 6 \quad 8 \quad 10 \]

\[ Q_{\text{in}} (fC) \]

\[ + \quad Q_{\text{th}}=0.5fC \]

\[ \times \quad Q_{\text{th}}=0.6fC \]

\[ \Delta \quad Q_{\text{th}}=0.7fC \]

\[ \square \quad Q_{\text{th}}=0.8fC \]

\[ \diamond \quad Q_{\text{th}}=0.9fC \]
TDC

Delay Locked Loop based TDC

- 32 bins, 97 ps width

Hit multiplexing

- Extensive simulation with realistic stimulus
  - 99.4% hits recorded, 0.6% hits collide, pile-up recorded

<table>
<thead>
<tr>
<th></th>
<th>Power [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DLL</td>
<td>20</td>
</tr>
<tr>
<td>Register bank</td>
<td>5</td>
</tr>
<tr>
<td>20x DLL + 40x banks</td>
<td>600 (14% of chip budget)</td>
</tr>
</tbody>
</table>
TDC floor planning and layout

- DLL
- Fine time register (lead)
- Encoder
- Fine time register (trail)
- Encoder

$300 \, \mu m$
Introduction

- NA62 Gigatracker
- TDCpix readout ASIC

Design of TDCpix

- Architecture
- Front-End
- TDC

Prototype ASIC

- Measured performances
Prototype ASIC

Folded 45x pixel column

Test pads

EoC

Pads

6.7 mm

2.8 mm
Prototype hybrid pixel assembly

Charge injection methods

- Electrical test pulse
- Focused IR laser
- Radioactive source
- Particle beam
Pixel performance

Uniform gain
- $72 \pm 1.5_{\text{RMS}} \text{ mV/fC}$

Pixel baseline distribution
- 50 mV peak to peak
- Trim circuit in the final TDCpix ASIC

Noise 180 e$^-$(ENC)
- $C_{\text{det}} = 250 \text{ pF}$

Discriminator jitter
- $<75 \text{ ps RMS (Q} > 2 \text{ fC}$

Charge injection with laser
300 V detector bias
TDC performance

TDC jitter

• < 10 ps RMS

Single hit timing resolution

• ~ 40 ps RMS

  \[ f_{\text{clk}} = 320 \text{ MHz}, \quad T_{\text{bin}} = 97.7 \text{ ps} \]
Full chain timing performance

$T_0$ RMS < 75 ps

- $Q > 2$ fC
  - Time walk correction included

- Charge injection with laser
  - Detector bias 300 V
  - Fixed position, pixel center
Timing particles in beam test

Four prototype assemblies

- Detection efficiency > 95%
  - Without threshold trimming

- Timing resolution < 175 ps RMS
  - 200 μm Si, 2.4 fC MPC
Timing resolution limit of sensor

Timing resolution
- Laser: 75 ps RMS
- Test beam: 175 ps RMS

Random fluctuations of input current signal shape
- Position of track hit in pixel
- Charge straggling

Ongoing studies
- Track hit position
  - Position scan with laser: 85 ps RMS
- Charge straggling
  - > 60 ps RMS
Summary

Design of TDCpix for the NA62 Gigatracker
- 45×40, 300×300 μm² pixels readout
- Time tagging of 130 Mevents/s

Measured performances of prototype ASIC
- 180 e⁻ ENC front end
- 75 ps discriminator jitter (Q > 2 fC)
- Low jitter and linear TDC, 40 ps timing resolution
- 75 ps RMS timing resolution for constant input pulse shape (Q > 2 fC)
- 175 ps RMS timing resolution with particles in beam test

Timing resolution dominated by random fluctuations of sensor current
Gigatracker stations

GTK 1

GTK 2

GTK 3

Cooling 0.18% $X_0$

TDCpix Front-End 100 $\mu$m 0.11% $X_0$

200 $\mu$m Si pixel sensor and bonds 0.24% $X_0$

Beam

TDCpix Front-End

Pixel chip

Sensor

Sn-Pb Bump Bond
Delay locked loop based TDC

320 MHz clock, 32 starved delay cells → 97 ps time bin.
Configuration and SEU

Serial configuration interface

- ~17000 configuration bits
- Double column daisy chains in pixel matrix

SEU

- Cross section $2 \cdot 10^{-14} \text{ cm}^2/\text{FF}$
- Flow 66 MHz/cm$^2$
- SEU rate: $2.24 \cdot 10^{-2} \text{ Hz}$

Triple Module Redundancy

- All configuration FFs, state machines, FIFOs and counters

- No TMR on data path registers
  - Data remain shortly on chip
Data serialization

Multiplexing of 4 groups of 10 columns
- 10 columns 27 Mhits/s
- Hit data word 48 bits
- 8b/10b encoding 60 bits

2.4 Gb/s serial transmitters
- Expected to use significant fraction of remaining power budget
Prototype EoC demonstrator ASIC

Pixel cells

Fine register (lead)
Fine register (trail)
Coarse reg (lead)
Coarse reg (fall)

Coarse counter

Hit arbiter
5:1 mux

Serial readout
320 Mb/s

DLL

Test pads

Folded 45x pixel column

EoC

Pads

6.7 mm

2.8 mm
Pixel performance

Uniform gain
- $72 \pm 1.5_{\text{RMS}}$ mV/fC

Pixel baseline distribution
- $1117 \pm 10.8_{\text{RMS}}$ mV
- Peak to peak: 50 mV
- Offset trim in the final TDCpix ASIC

Noise 180 e$^-$ (ENC)
- Bonded to detector $C_{\text{det}} = 250$ pF

Discriminator jitter
- $< 75$ ps RMS (Q > 2 fC)

Charge injection with laser
300 V detector bias
75 ps
TDC performance

TDC jitter
- < 10 ps RMS

Single hit timing resolution
- ~ 40 ps RMS
  - $f_{\text{clk}} = 320$ MHz, $T_{\text{bin}} = 97.7$ ps
  - Correcting for non-linearity 30 ps