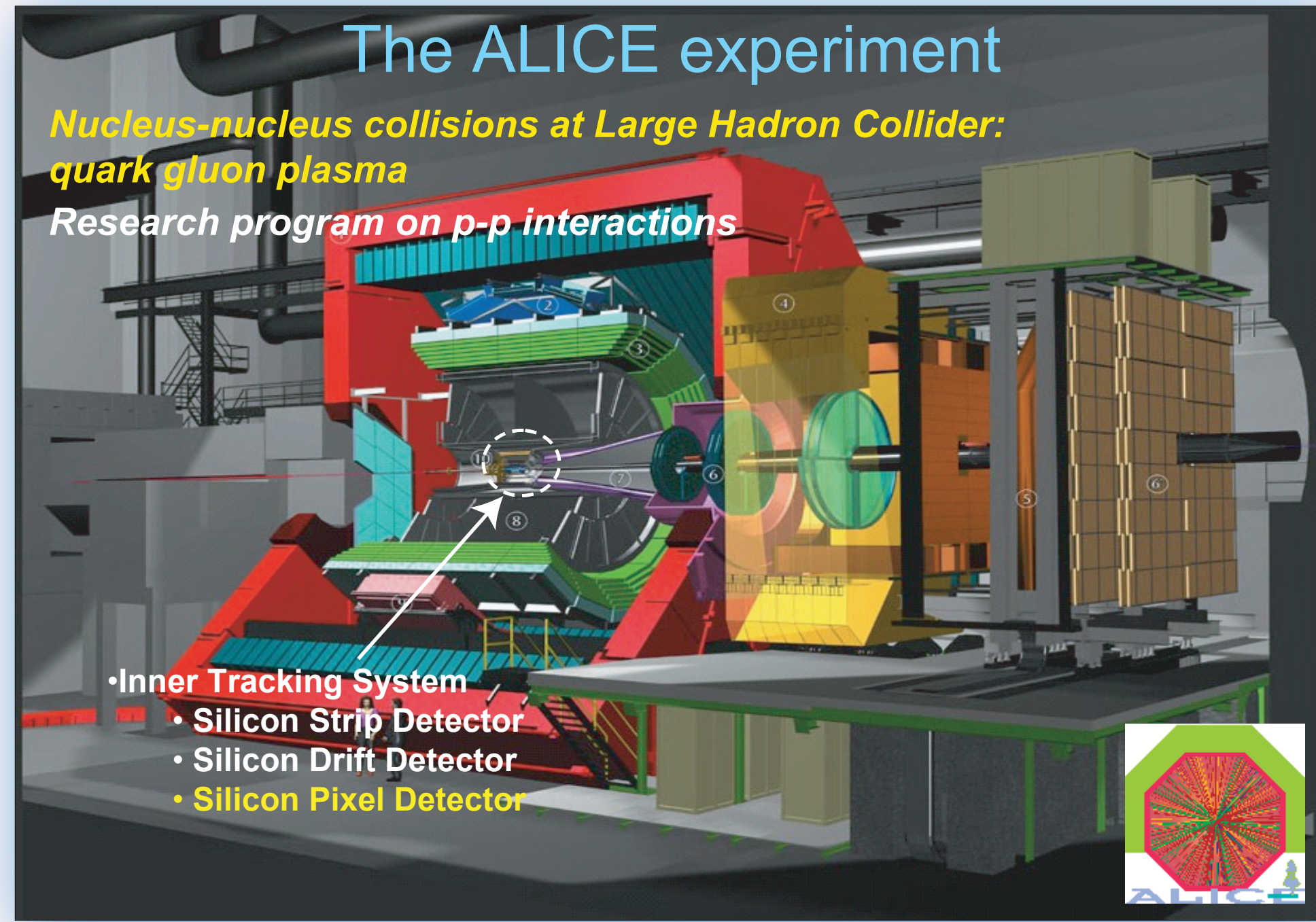# The Level 0 Pixel Trigger System for the ALICE experiment
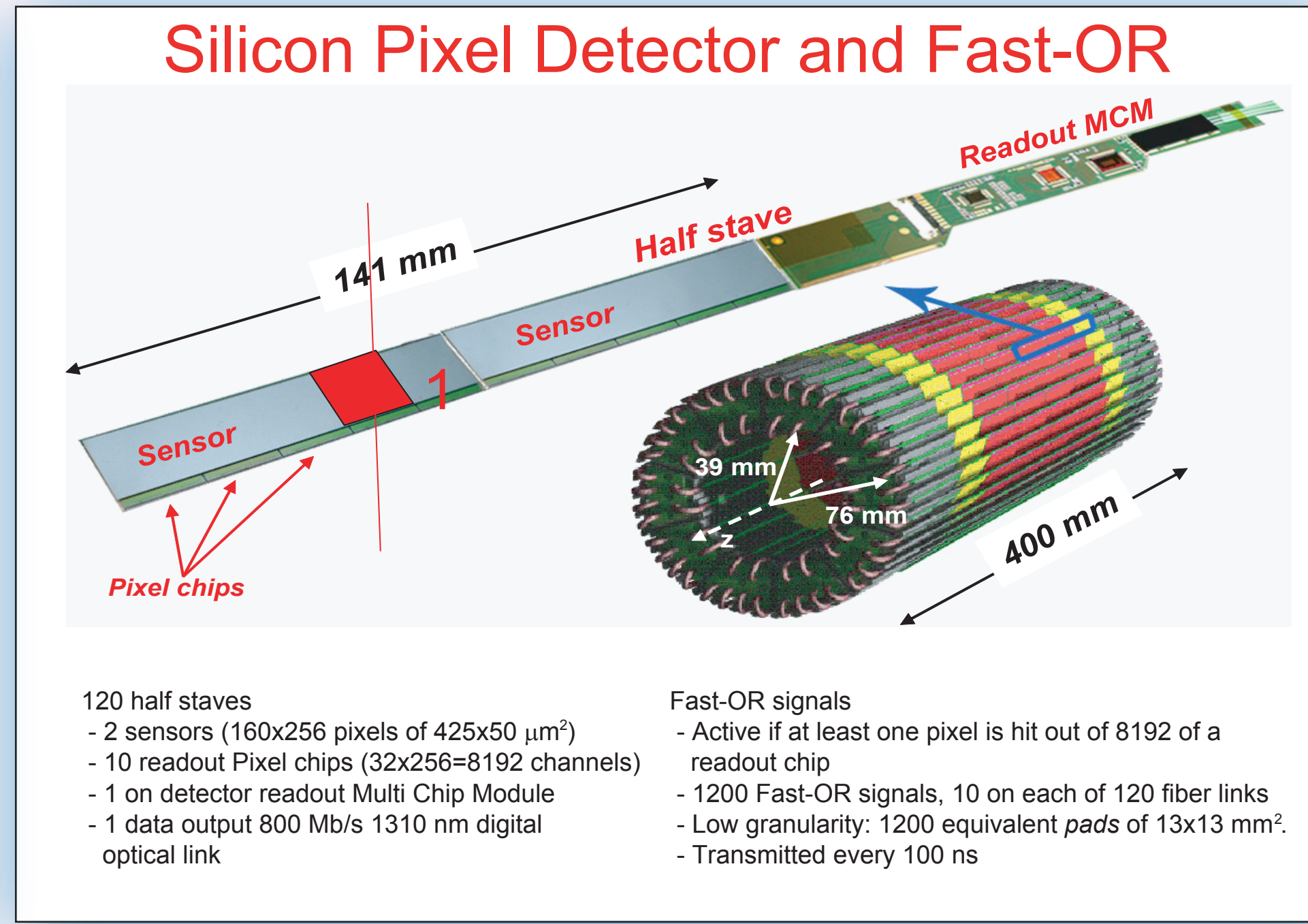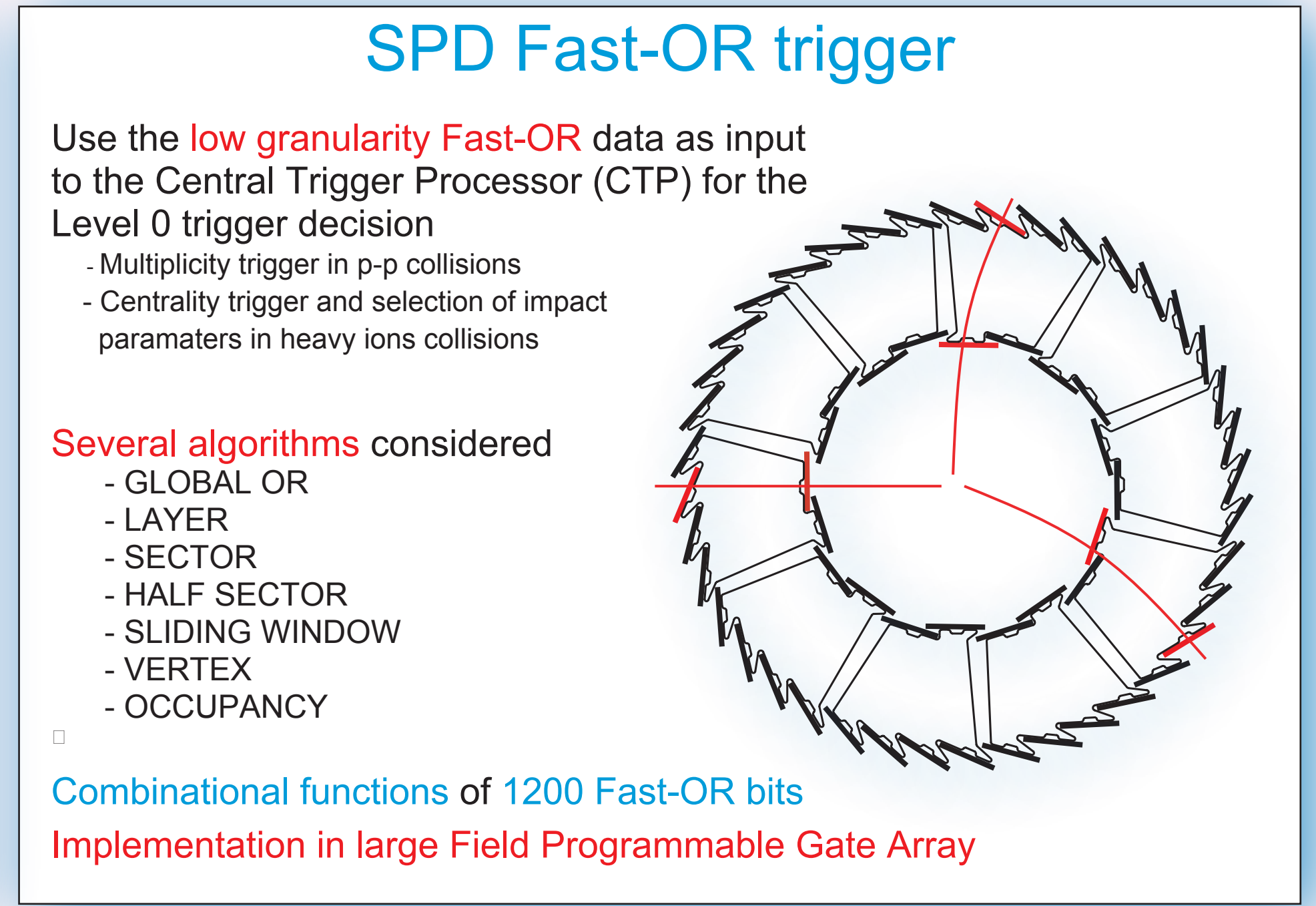
ABSTRACT

The ALICE Silicon Pixel Detector contains 1200 readout chips. Each chip provides a digital Fast-OR output signal to indicate the presence of at least one pixel hit among the 8192 pixels of its readout matrix. The 1200 bits are transmitted every 100 ns on 120 data readout optical links using the G-Link protocol. The Pixel Trigger System extracts and processes them to deliver an input signal to the Level 0 trigger processor, within a latency of 800 ns. The system is modular and based on FPGA devices. The architecture allows the user to define and implement various trigger algorithms. The system uses advanced 12-channel parallel optical fiber modules operating at 1310 nm as optical receivers. Multi-channel G-Link receivers were realized in programmable hardware and tested. The design of the system and the progress of the ALICE Pixel Trigger project are described in this poster.

The ALICE experiment

Nucleus-nucleus collisions at Large Hadron Collider: quark gluon plasma

Research program on p-p interactions

- Inner Tracking System
  - Silicon Strip Detector
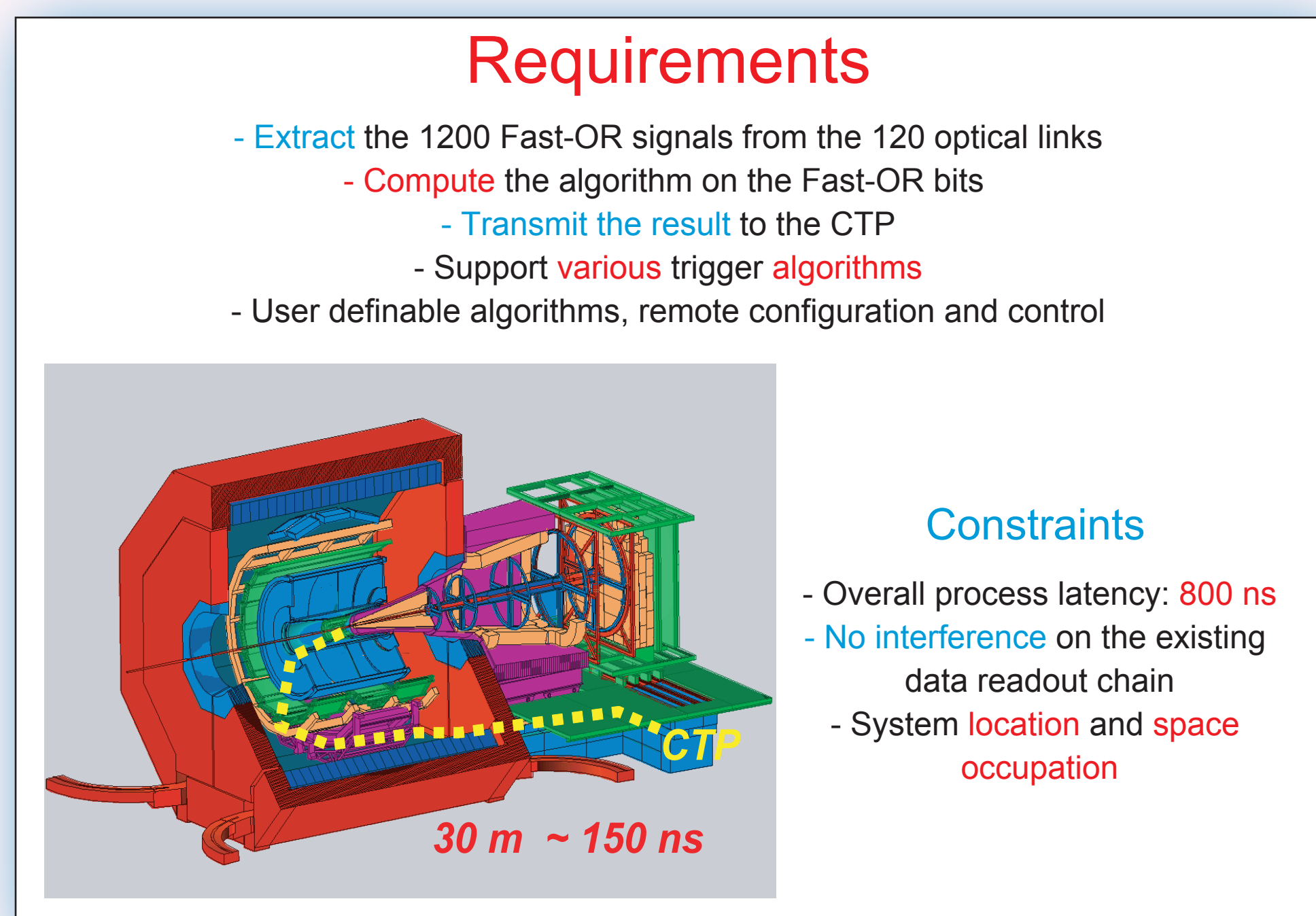 - Silicon Drift Detector
  - Silicon Pixel Detector

ALICE is an experiment designed to study the physics of strongly interacting matter and the properties of quark gluon plasma in the collisions between heavy ions nuclei at the Large Hadron Collider (LHC) at CERN [1]. The ALICE apparatus allows particle identification over a broad momentum range, powerful tracking and good resolution from 100 MeV/c to 100 GeV/c and excellent determination of secondary vertices. These features allow important contributions also to the physics of proton-proton interactions. The low material budget and the moderate magnetic field make the apparatus suited for studying low transverse momentum phenomena in proton-proton collisions.

Silicon Pixel Detector and Fast-OR

120 half staves
- 2 sensors (160x256 pixels of 425x50 µm²)
- 10 readout chips (32x256=8192 channels)
- 1 on detector readout Multi Chip Module
- 1 data output 800 Mb/s 1310 nm digital optical link

Fast-OR signals
- Active if at least one pixel is hit out of 8192 of a readout chip
- 1200 Fast-OR signals, 10 on each of 120 fiber links
- Low granularity: 1200 equivalent pads of 13x13 mm².
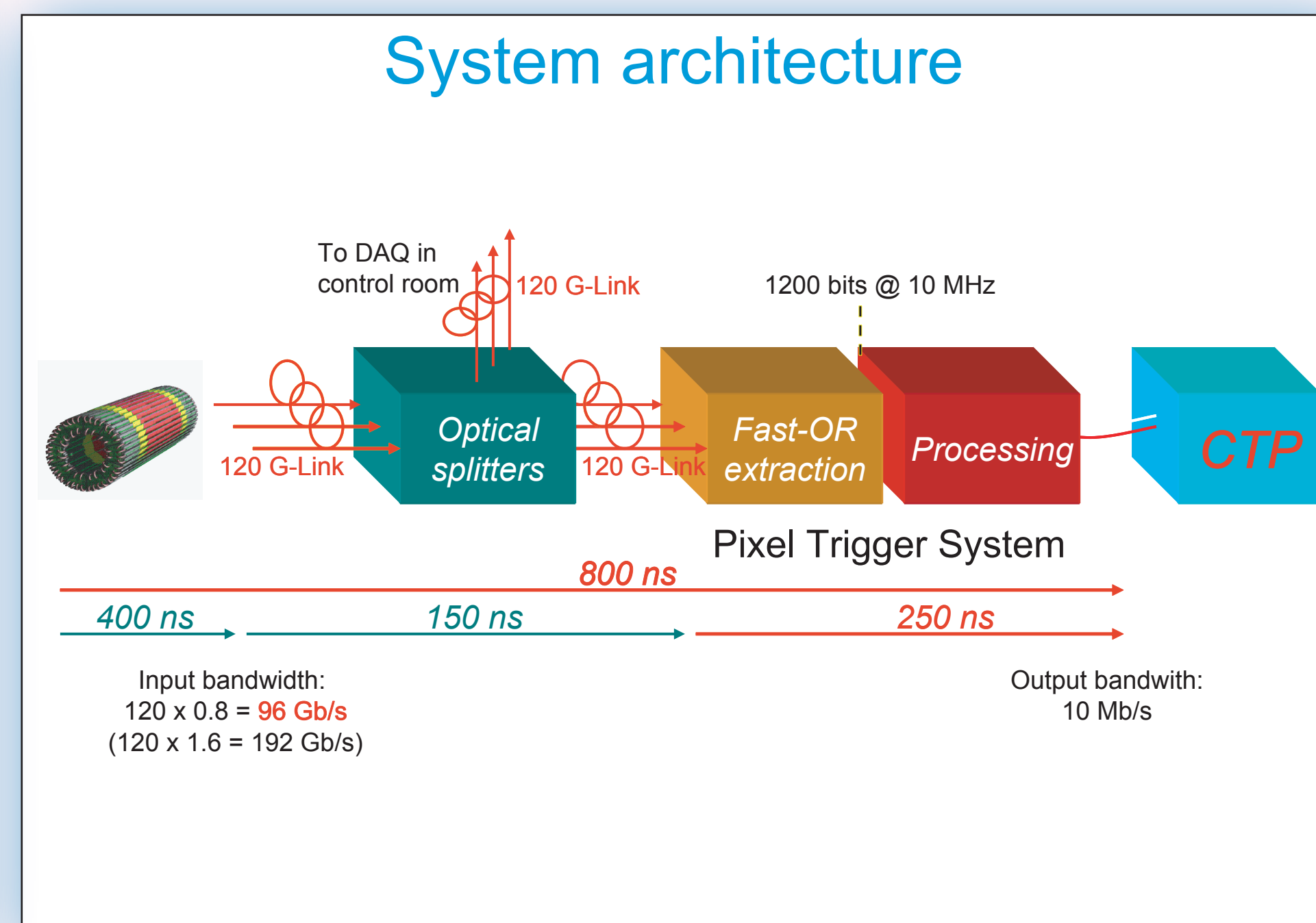- Transmitted every 100 ns

The ALICE Silicon Pixel Detector (SPD) is a double layer barrel pixel detector [2]. It is made up of 120 half staves, 40 in the inner layer and 80 in the outer one. One half stave comprises two 200 mm thick silicon pixel sensors. Each sensor has a matrix of 160x256 pixels of 425x50 µm². A sensor is bump bonded to 5 mixed signal readout chips (0.25 µm CMOS). The array of 10 pixel chips in each half stave is read out via a Multi Chip Module (MCM) [3]. Data are transmitted at 800 Mb/s on an optical link with a wavelength of 1310 nm using the G-Link protocol [4]. The readout of the hit data, stored in the readout chips memory, is initiated at the reception of a Level 2 trigger signal.
The 1200 readout chips of the SPD feature a digital Fast-OR output signal. This is active when at least one of the 8192 channels of the chip records a hit. The 10 Fast-OR bits of each half stave are transmitted every 100 ns on the output link. The Fast-OR signals allow the SPD to be operated as a low latency and low granularity pad detector.

SPD Fast-OR trigger

Use the **low granularity Fast-OR data** as input to the **Central Trigger Processor (CTP)** for the **Level 0** trigger decision
- Multiplicity trigger in p-p collisions
- Centrality trigger and selection of impact paramaters in heavy ions collisions

Several algorithms considered
- GLOBAL OR
- LAYER
- SECTOR
- HALF SECTOR
- SLIDING WINDOW
- VERTEX
- OCCUPANCY

Combinational functions of 1200 Fast-OR bits
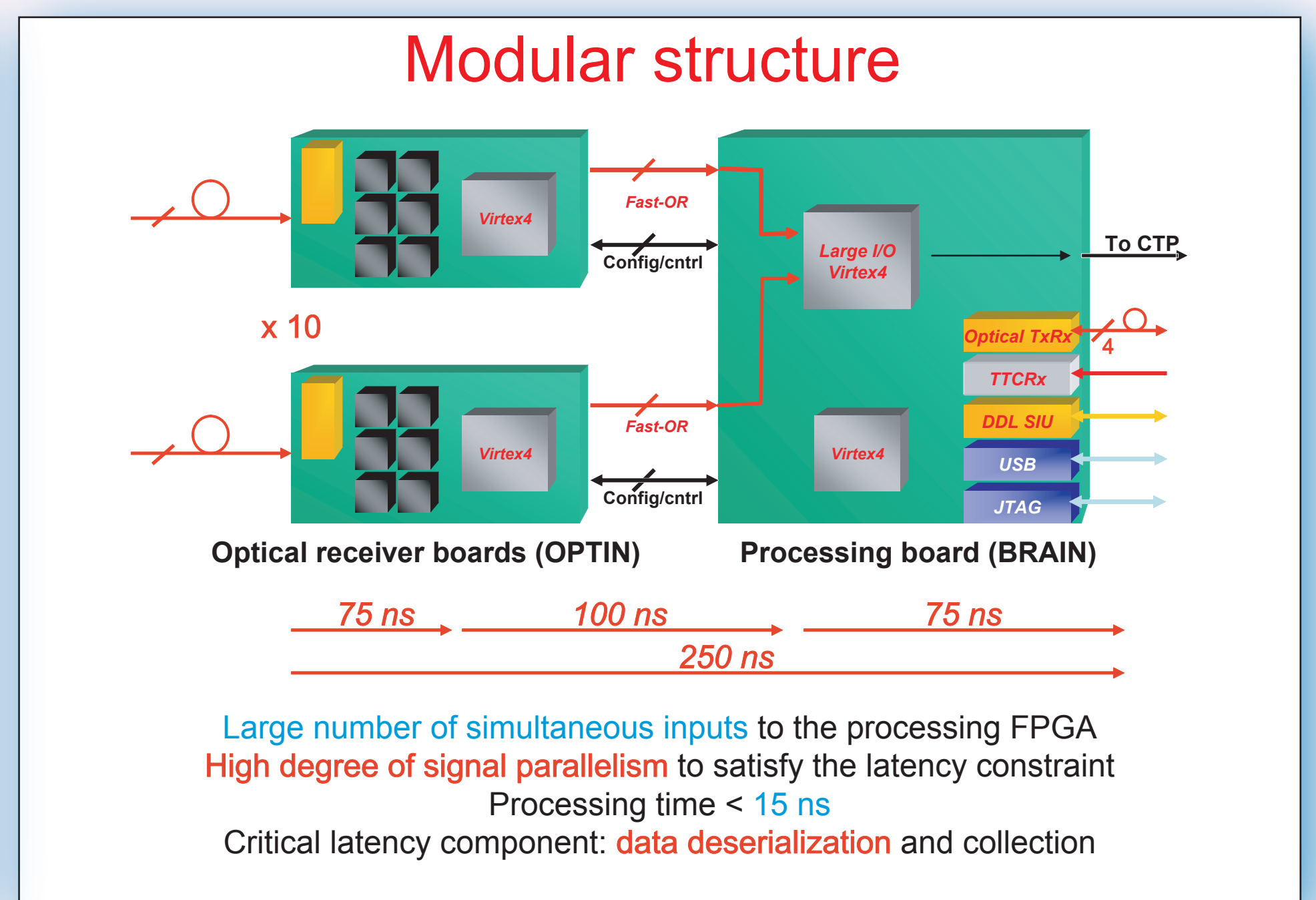**Implementation** in large Field Programmable Gate Array

The 1200 Fast-OR signals will be used to generate an input signal for the Level 0 trigger decision in the ALICE Central Trigger Processor (CTP) [5]. Various trigger algorithms taking into account the Fast-OR data have been investigated [6], including topology based and occupancy based ones. Event selection in heavy ions runs and background rejection in proton-proton interactions can be significantly improved using the Fast-OR data. The different algorithms can be implemented as combinational logic functions of the 1200 Fast-OR signals. This naturally suggests an implementation of the algorithm on a programmable hardware device.

Requirements

- **Extract** the 1200 Fast-OR signals from the 120 optical links
- **Compute** the algorithm on the Fast-OR bits
- **Transmit** the result to the CTP
- Support **various** trigger **algorithms**
- User definable algorithms, remote configuration and control

Constraints

- Overall process latency: **800 ns**
- **No interference** on the existing data readout chain
- System **location** and **space** occupation

30 m ~ 150 ns

The Pixel Trigger System for the ALICE experiment is required to extract and process the 1200 Fast-OR signals in order to provide a signal input to the Level 0 trigger decision in the CTP. Various user selectable processing algorithms shall be supported by the hardware platform. The overall time latency of the process is required to be less than 800 ns from the interaction time to the input to the CTP. This requires the system to be located as close as possible to the detector and the CTP. A limited space of one standard crate could be allocated in the electronic racks next to the CTP.
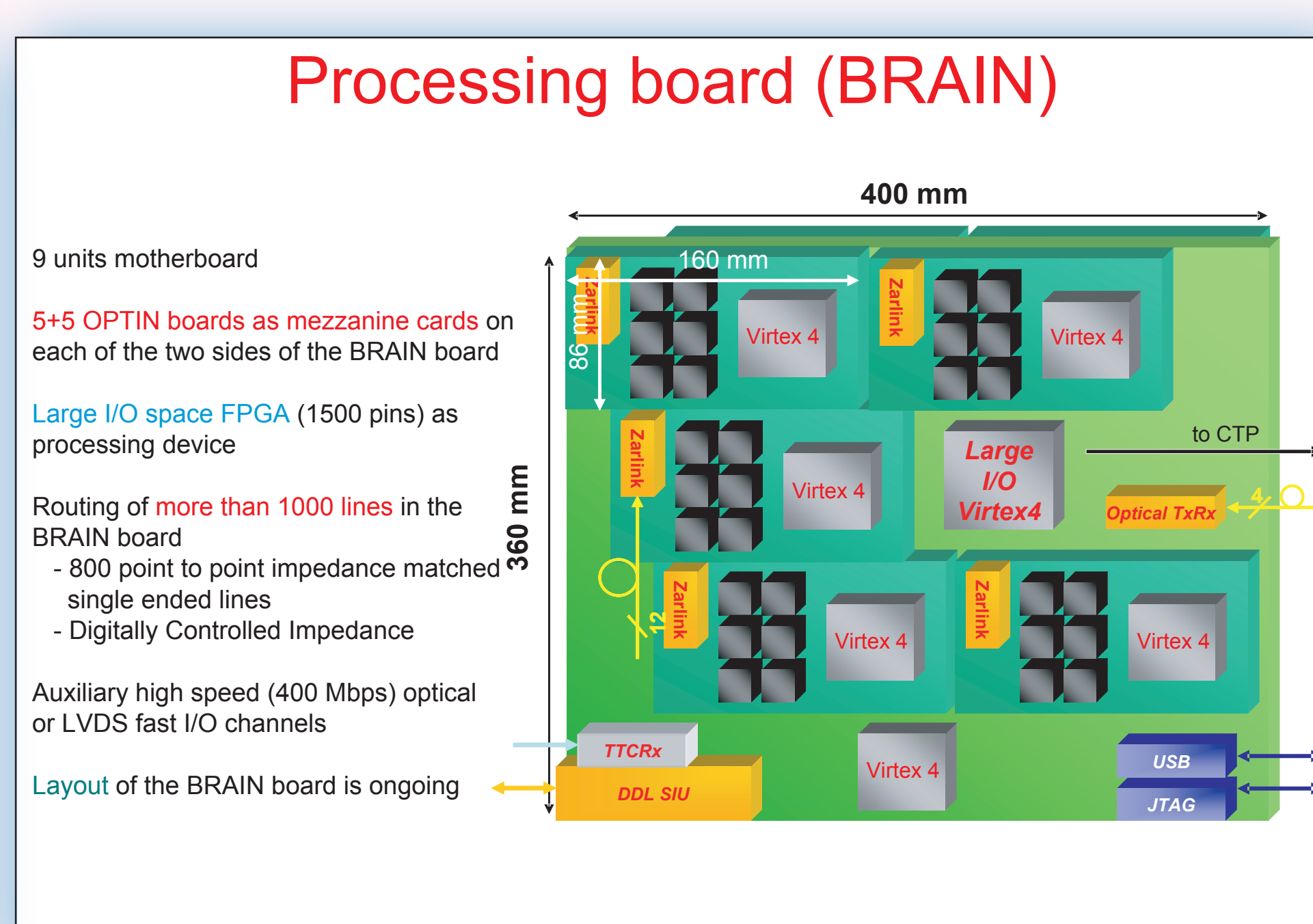
System architecture

Pixel Trigger System

800 ns

400 ns | 150 ns | 250 ns

Input bandwidth:
120 x 0.8 = **96 Gb/s**
(120 x 1.6 = 192 Gb/s)

Output bandwith:
10 Mb/s

The 120 optical fibers coming from the detector are connected to a commercial passive optical splitter located close to the CTP. The splitter output fibers forward the data to the SPD readout electronics and to the electronic boards of the Pixel Trigger system, located in the same rack of the splitter. The data readout remains fully independent from the Pixel Trigger System.
The Pixel Trigger electronics is subdivided in two subsystems. The first one deserializes the data and extracts the 1200 Fast-OR bits. The second one implements the processing algorithm on the 1200 input bits and generates the output signal for the CTP. The former architecture is naturally suggested by the need of providing all the 1200 Fast-OR bits as simultaneous inputs to the processing unit.

Modular structure

Optical receiver boards (OPTIN) | **Processing board (BRAIN)**

75 ns | 100 ns | 75 ns
250 ns

Large number of simultaneous inputs to the processing FPGA
High degree of signal parallelism to satisfy the latency constraint
Processing time < **15 ns**
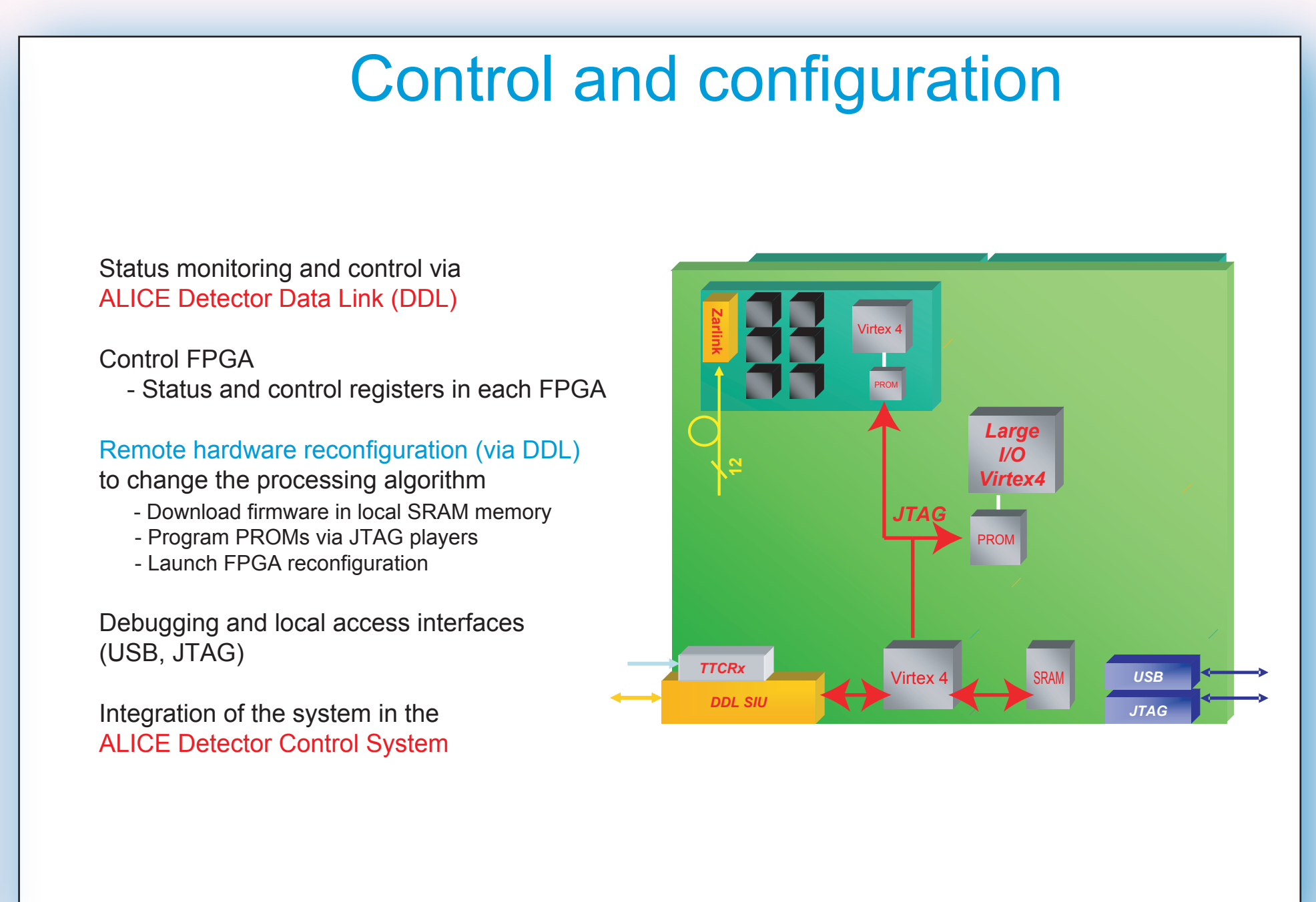Critical latency component: **data deserialization** and collection

The overall latency budget of 800 ns can be subdivided among each of the processes along the data flow. The on-detector electronics takes 400 ns from the collision to transmit the Fast-OR bits. The 30 m optical fibers path length from the detector to the system implies a signal delay of 150 ns. Therefore only 250 ns can be allocated to the deserialization, extraction and processing phases.
The algorithm to process the 1200 Fast-OR bits will be implemented in programmable hardware to allow fast execution, upgrading and reconfiguration by the user. The implementation on a large FPGA of some of the proposed trigger algorithms has been simulated. Even the most complex function can be processed in less than 15 ns in a Xilinx Virtex 4 device. The critical delays in the system are therefore associated with the Fast-OR data deserialization, extraction and transfer between the peripheral FPGAs and the processing unit.

OPTIN board

- Virtex 4 LX 60
- HDMP-1034
- Zarlink Optical module
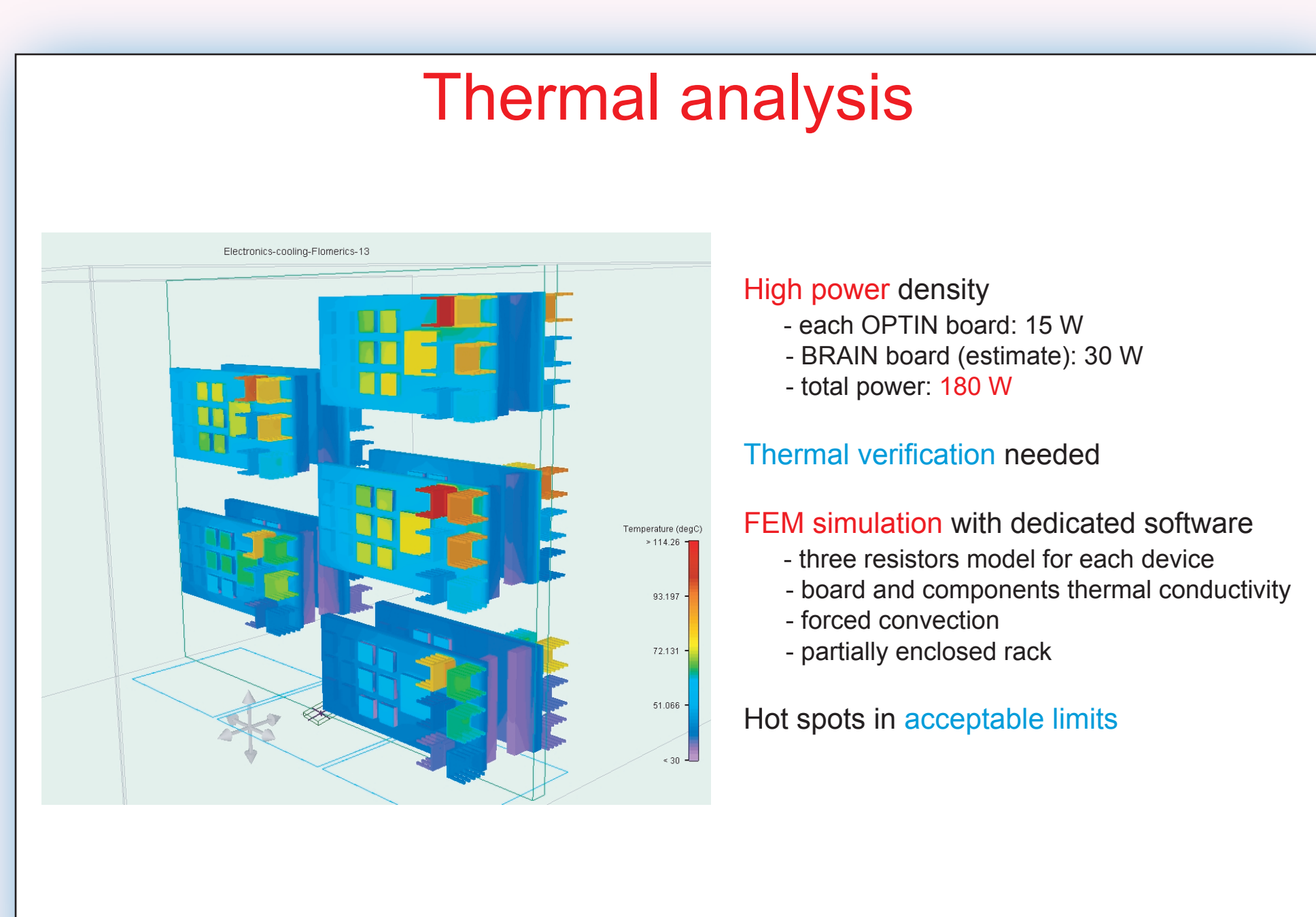- cPCI Connectors
- 84mm / 160 mm
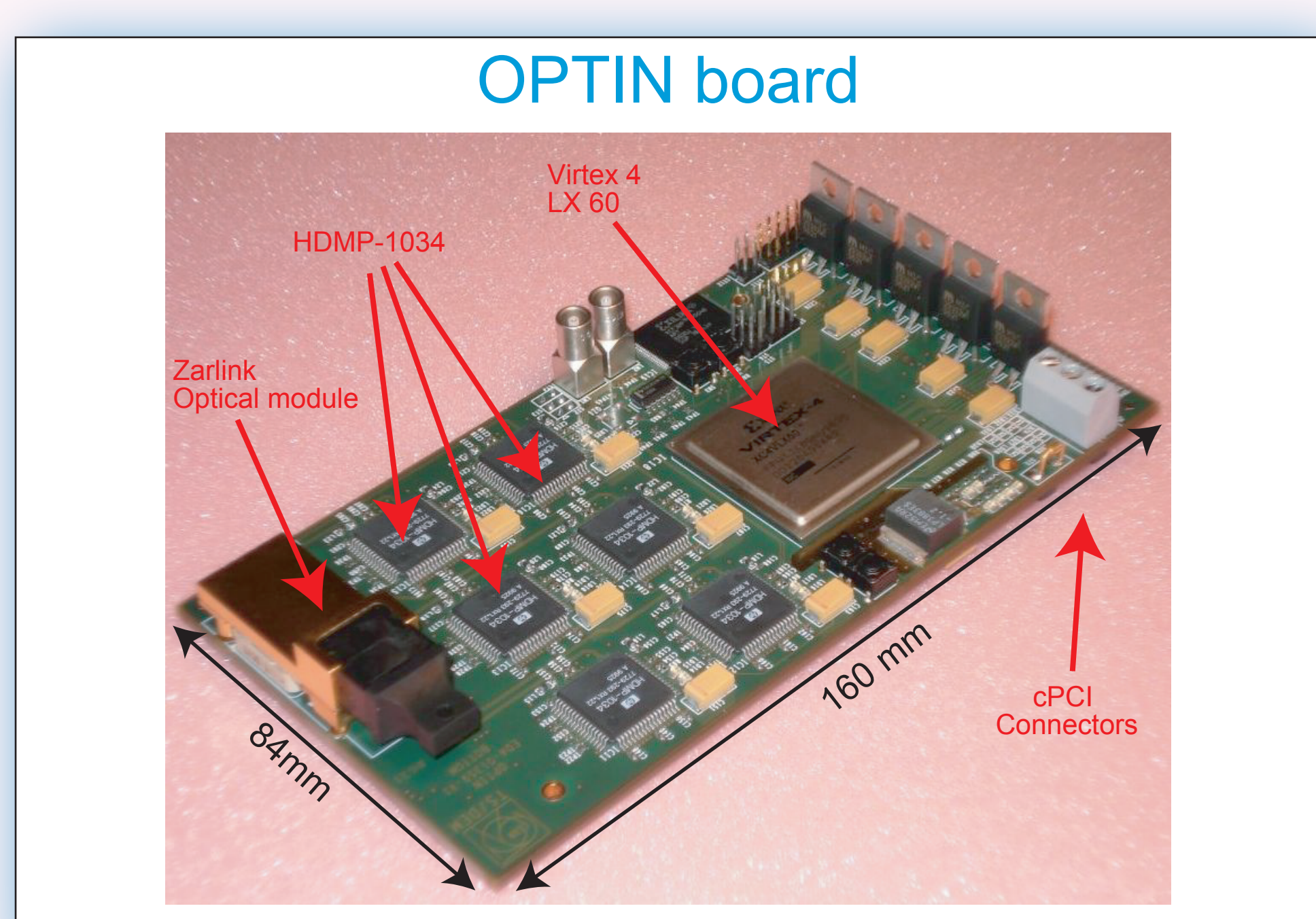
The OPTIN board has been designed and the first prototype produced and tested. It is a 12 layer printed circuit board. It has four connectors compatible with the IEEE 1386 Common Mezzanine Card standard. However, the board is larger than the envelope specified in the standard. Each OPTIN board extracts the Fast-OR signals of 12 optical channels among the 120 arriving from the detector. One Zarlink optical module receiver converts and amplifies the signals received on the incoming 12 fiber bundle. Twelve Agilent HDMP-1034 deserialize and realign the data streams. A Xilinx Virtex 4 LX60 FPGA receives the parallel outputs of the deserializers, extracts the 120 Fast-OR bits received every 100 ns and re-transmits them on a dedicated parallel output bus. Ten OPTIN boards in total are needed for the full system.

Processing board (BRAIN)

9 units motherboard

5+5 OPTIN boards as mezzanine cards on each of the two sides of the BRAIN board

Large I/O space FPGA (1500 pins) as processing device

Routing of **more than 1000 lines** in the BRAIN board
- 800 point to point impedance matched single ended lines
- Digitally Controlled Impedance

Auxiliary high speed (400 Mbps) optical or LVDS fast I/O channels
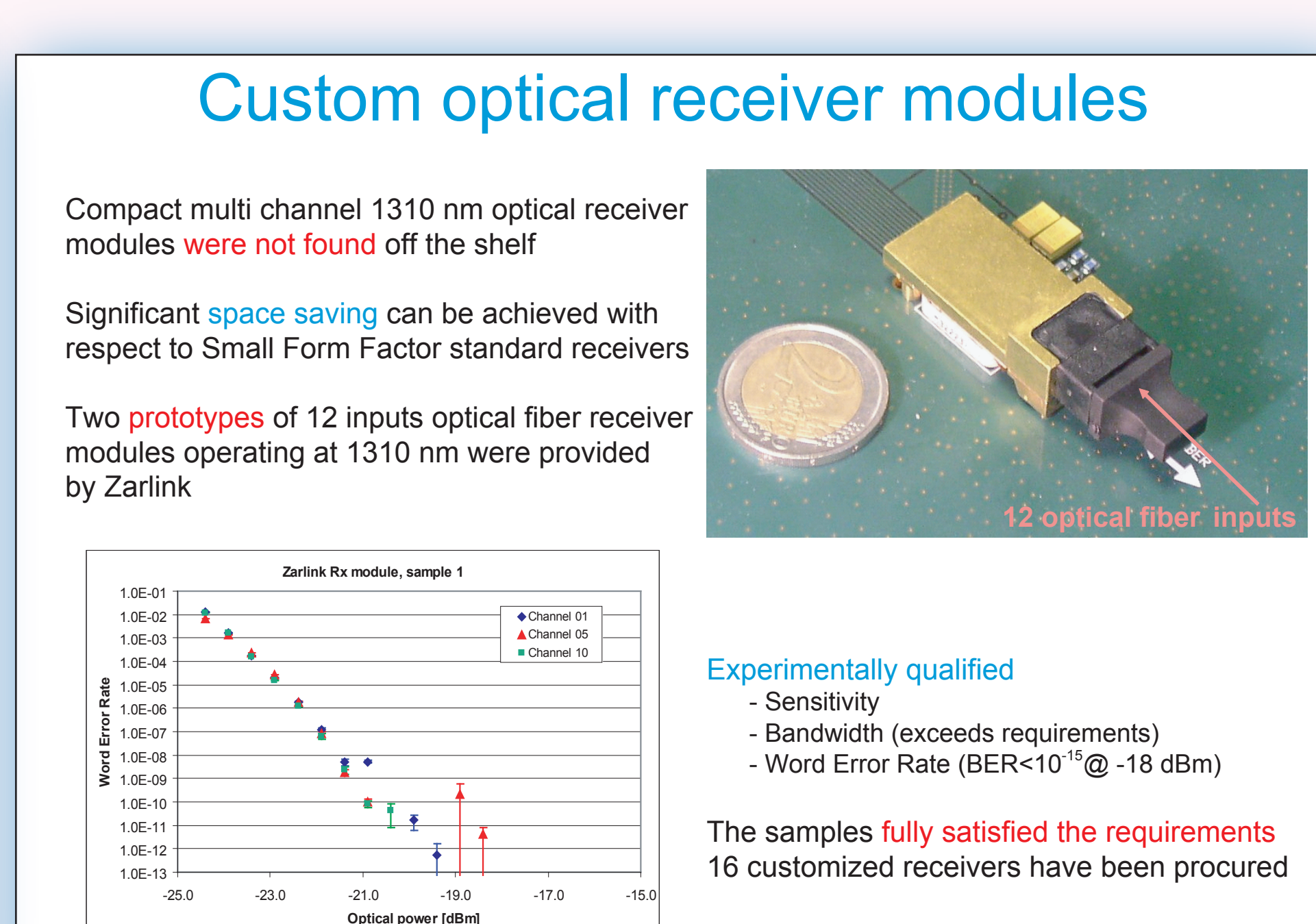
Layout of the BRAIN board is ongoing

The processing board (BRAIN) is a large electronic board. Most of its area is reserved to connect 10 OPTIN boards as mezzanine cards, 5 on each side. This interconnection solution is made possible by the compact design of the OPTIN board. The routing of the signals between the boards is flexible, avoiding the need of a backplane or wired interconnections. A large I/O space FPGA is the core of the BRAIN board. A Xilinx Virtex 4 LX100 with 1513 pins has been chosen as the processing device because of the large number of parallel lines needed to receive the Fast-OR bits from the OPTIN boards with a minimum latency. There are 64 Fast-OR output lines on each OPTIN board. The 1200 Fast-OR bits are transferred at Double Data Rate (80.16 MHz) on a dedicated bus of 640 lines connected to the processing FPGA.

Control and configuration

Status monitoring and control via **ALICE Detector Data Link (DDL)**

Control FPGA
- Status and control registers in each FPGA

Remote hardware reconfiguration (via DDL) to change the processing algorithm
- Download firmware in local SRAM memory
- Program PROMs via JTAG players
- Launch FPGA reconfiguration

Debugging and local access interfaces (USB, JTAG)

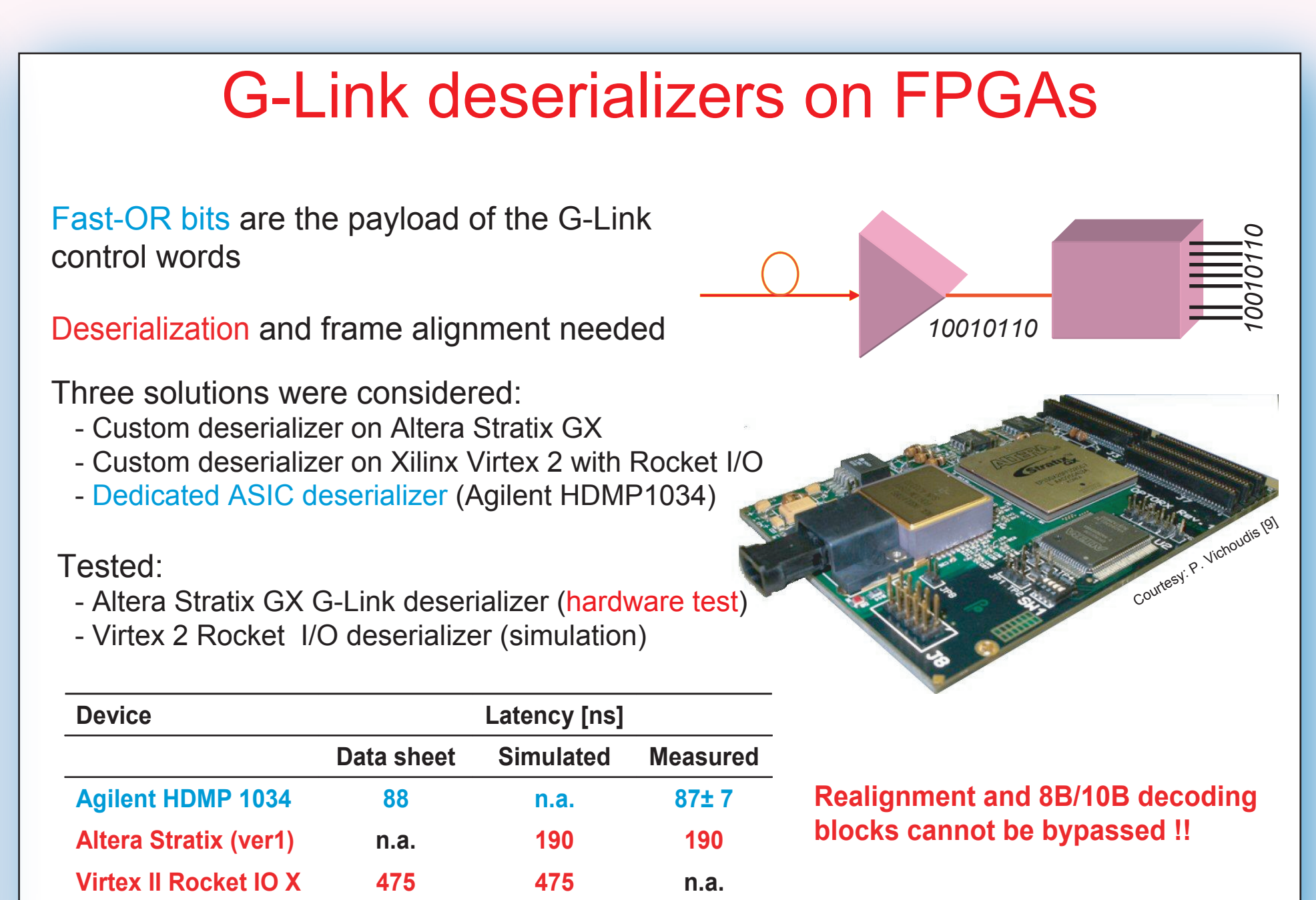Integration of the system in the **ALICE Detector Control System**

Full integration of the Pixel Trigger system in the ALICE Detector Control System is mandatory. The control is via the ALICE DDL interface. A second FPGA (Virtex 4 LX 40) is dedicated to the slow control, to the system interfaces and to implement the reconfiguration of the main processing FPGA. Status monitoring and control are implemented via status and configuration registers in all the programmable devices of the system accessed by a local bus. The processing FPGA can be reprogrammed remotely. The programming file for a given processing algorithm is downloaded via the DDL link and the control FPGA to local SRAM memory. The control device then transfers by JTAG the configuration bitstream into the Flash PROM connected to the processing FPGA. Reconfiguration of the latter one is finally launched via a JTAG command.

Thermal analysis

High power density
- each OPTIN board: 15 W
- BRAIN board (estimate): 30 W
- total power: **180 W**

Thermal verification needed

FEM simulation with dedicated software
- three resistors model for each device
- board and components thermal conductivity
- forced convection
- partially enclosed rack

Hot spots in **acceptable limits**

The total power consumption is 180 W. The density of the dissipated power is high and thermal verification of the design was required. A finite element heat flow simulation of the system was implemented at CERN using dedicated software tools [7]. Detailed thermal models and geometry of the components and of the boards of the system were considered. The boards were located in the partially enclosed volume of an electronic rack, with no other boards in the adjacent slots as it is foreseen for the real case. The simulation considered forced air convection. The hot spots are the voltage regulators on the OPTIN boards. The model showed that their temperature is below ratings. Worst case conditions were assumed at each step in the definition of the thermal model.

Custom optical receiver modules

Compact multi channel 1310 nm optical receiver modules **were not found** off the shelf

Significant **space saving** can be achieved with respect to Small Form Factor standard receivers

Two **prototypes** of 12 inputs optical fiber receiver modules operating at 1310 nm were provided by Zarlink

12 optical fiber inputs

Experimentally qualified
- Sensitivity
- Bandwidth (exceeds requirements)
- Word Error Rate (BER<10⁻¹⁵ @ -18 dBm)

The samples **fully satisfied the requirements**
16 customized receivers have been procured

Parallel optical fiber modules integrate an array of photodiodes and a receiver chip in a single device. Engineering samples of parallel optical fiber modules operating at 1310 nm were provided to our group by a private company (Zarlink). The performance of the two samples was experimentally evaluated with respect to sensitivity, bandwidth, overall jitter and transmission error rate. For these measurements an optical communication setup [8] was used. The rate of frame (20 bit word) errors in the transmission was measured at various optical power levels. This figure allowed an estimation of a bit error rate lower than 10⁻¹⁵ at -18 dBm. The Zarlink parallel optical fiber module was therefore chosen for the Pixel Trigger system.

G-Link deserializers on FPGAs

Fast-OR bits are the payload of the G-Link control words

Deserialization and frame alignment needed

Three solutions were considered:
- Custom deserializer on Altera Stratix GX
- Custom deserializer on Xilinx Virtex 2 with Rocket I/O
- **Dedicated ASIC deserializer** (Agilent HDMP1034)

Tested:
- Altera Stratix GX G-Link deserializer (**hardware test**)
- Virtex 2 Rocket I/O deserializer (simulation)

Device	Latency [ns]		
	Data sheet	Simulated	Measured
Agilent HDMP 1034	88	n.a.	87± 7
Altera Stratix (ver1)	n.a.	190	190
Virtex II Rocket IO X	475	475	n.a.

Realignment and 8B/10B decoding blocks cannot be bypassed !!

Latest generation of FPGAs feature modules for serial communication up to few Gb/s including serializer/deserializers, comma alignment blocks and protocol decoders. These modules are implemented on dedicated circuitry on the FPGA chip. The implementation of a multichannel G-Link deserializer/receiver on FPGAs with fast serial circuitry was investigated. A 12-channel G-Link receiver was implemented in HDL. Its realizatioon a Xilinx Virtex 2 with Rocket I/O X was simulated. A real circuit was implemented using a parallel optical receiver board based on an Altera Stratix GX and developed at CERN [9] by the CMS-ECAL group. This was to our knowledge the first parallel multi-channel G-Link receiver on programmable hardware. The latencies of the FPGA based circuits were significantly higher than the one offered by the dedicated ASIC Agilent HDMP-1034 because several functional blocks of the FPGA dedicated circuitry cannot be bypassed. The latency constraint on the Pixel Trigger system was not compatible with the performances of the FPGA based circuits. The HDMP-1034 was chosen for the receiver cards of the Pixel Trigger system.

G. Aglieri Rinella, CERN PH/ED Fellow, ALICE Silicon Pixel Project. email: gianluca.aglieri.rinella@cern.ch. On behalf of the ALICE Silicon Pixel Detector project.

References: [1] ALICE Collaboration, ALICE Physics Performance Report, CERN-LHCC-2003-049, J. Phys., G 30 (2004) 1517-1763. **[2]** P. Riedler et al., Overview and status of the ALICE Silicon Pixel Detector, Proceedings of the Pixel 2005 Conference, Bonn, Germany. **[3]** A. Kluge, The ALICE silicon pixel detector front-end and read-out electronics, Nucl. Instr. and Meth., A 560 (2006) 67-70. **[4]** Agilent Technologies, Low Cost Gigabit Rate Transmit/Receive Chip Set with TTL I/Os, Technical Data, HDMP-1022/HDMP-1024 data sheet, December 2003. **[5]** G. Aglieri Rinella et al., The Level 0 Pixel Trigger System for the ALICE experiment, Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments, LECC 2006, Valencia. **[6]** J. Conrad et al., Minimum Bias Triggers in Proton-Proton Collisions with the VZERO and Silicon Pixel Detectors, Alice Internal Note, ALICE-INT-2005-025. **[7]** E. Dupont, Electronics cooling with FLOTHERM: the Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector, CERN TS, CFD-2006-05, June 2006. **[8]** G. Aglieri Rinella, Characterization of two Zarlink 1310 nm 12 channels optical receiver modules, ALICE Internal note ALICE-INT-2006-025. **[9]** S. Reynaud and P. Vichoudis, A multi-channel optical plug-in module for gigabit data reception, Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments, LECC 2006, Valencia. Acknowledgements: A. Singovski, F. Vasey, P. Vichoudis. Printed: **November 2006**.